Test and optimization of a two-phase thermosyphon cooling system for microprocessors under real working conditions

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Abstract:
The present work features the test and optimization of a two-phase thermosyphon cooling system for microprocessors. Microcavities arrays are structured on the thermosyphon hot surface, for nucleate pool boiling enhancement. The inter-cavity distance, *S* is the tested parameter with surfaces ranging from *S* = 100 µm to 600 µm and a smooth surface as reference. This set of surfaces is tested both for a horizontal and a vertical surface orientation, at steady-state and transient conditions. The working fluid is 3M's Novec HFE-7000, a dielectric engeneering fluid. Results have shown that smaller *S* resulted in lower wall superheat for both orientations, while cavities promoted an earlier onset of pool boiling. For the vertical oriented prototype, results account the heat transfer coefficient improvement to be stronger and correlated with a reducing *S*. Optimal results were obtained with the smallest parameter, *S* = 100 µm, suggesting further research with smaller *S* parameters. The final proof of concept application on a real processor was successfully demonstrated, with an average 5°C reduction and a lower thermal response time than the conventional cooling fan, during stress test.

Keywords: Thermosyphon, CPU cooling, pool boiling, micro-cavities, heat transfer coefficient enhancement, product development.

1. Introduction

Since the very first emergence of the transistor, processors have gone through a continuously growing development, either at its shape and size, or at the number of transistors they contain. In 1965, Gordon Moore, co-founder of Intel®, foresaw the number of transistors in an integrated circuit (IC) would approximately double every 2 years (Moore's Law, [1]). These predictions have held true up to today, and became one of the driving principles of the semiconductor industry. Today we have devices which exceed thousands of millions of transistors. However, Gordon Moore himself [1] has pointed out a thermal management issue, raising the question to whether it will or not be possible to remove the heat from tens of thousands of components in a single silicon chip. He argued that, due to the two-dimensionality of these chips, there will be an available surface for cooling close to each centre of heat generation (transistors). As we move towards billion transistor microprocessors, the growing power dissipation of these chips must be conveniently addressed. With ever-increasing chip heat fluxes, new cooling solutions have been developed during the past couple of decades, such as microchannel cooling, impingent liquid jet cooling, liquid spray cooling, immersion cooling, thermosyphons and vapour chambers. These technologies share a high heat flux absorption rates at low temperature variation, benefitting from phase change latent heat of vaporization, being two-phase cooling technologies. However, some exhibit quite a complex implementation approach while others are more practical and affordable. The thermosyphon is a simple system, yet very efficient due to the high heat exchange potential at a fully developed nucleate pool boiling regime, and it is sustainable, requiring no pumping power and only an electric fan. With the choice of a thermosyphon for the current work, this work proceeds the previous efforts by Moura within his master's thesis project [2], on the design and development of a pool boiling thermosyphon CPU cooling system. As he took the first steps in the development of the proposed product, going through the first stages of functional design, this work now follows it further into the test and optimization phases, as well as improving some design concepts.

1.1. Objective

The work comprises several tasks which are divided in two major parts, being the first a systematic study concerning the characterization of the thermosyphon's evaporator component by evaluating the Critical Heat Flux (CHF) and Heat Transfer Coefficient (*h*) achieved for each configuration, when the surfaces of the evaporator are micro-structured. The micro-structured test surfaces are composed by regular square matrix patterned cavities, etched by laser, with a fixed size and depth. The tested parameter is *S*, the distance between cavities [3]. Following the results reported in [2], [3], numerous micro-structured surfaces will be tested, to identify the distance between cavities allowing the highest CHF and *h*, thus leading to the lowest absolute thermal resistance. Preliminary tests will be performed for the evaporator working on the horizontal position, but the remaining will mainly address a

configuration in which the evaporator is fixed in the vertical position. This study will provide the best performing micro-pattern and design modifications to adapt the evaporator to the new orientation. Finally, in the second part of this work the system will be tested in a processor working under real conditions. For this part of the work the candidate will consider the assembly of the improved system to a real processor and evaluation of its cooling performance under typical and full CPU load real working conditions.

2. Design and optimization of the thermosyphon system

2.1. Horizontally oriented experimental facility

The facility considered in the present work and following the thermosyphon methodology consists of an evaporator, where heat is absorbed from the environment through a hot surface, and a condenser, where this heat is returned to the environment. The working fluid flows inside these elements in a closed loop. It is a two-phase system, with both liquid and vapour phases constantly present within the loop. An initial prototype was developed with excessive evaporator size, for later tests and size optimization. The implemented final facility is shown below in figure 2.1, featuring the evaporator in its lower region and the condenser on top. Two clear rubber pipes connect the two components. The evaporator is mounted on a Teflon base block, for insulated heat transfer and structural purposes. The transistor is mounted under the Teflon block, through an inner central cavity opening way to the copper surface's bottom. The condenser was designed following a reflux flow approach, as suggested by project peers who believed this approach could improve the efficiency of the cooling system. Later results show this statement depends on some other factors, although the final outcome confirms the proposed thesis. In fact, following a design point-of-view, the reflux condenser enables an overall more compact product, good for fitting inside the desktop computer to cool.

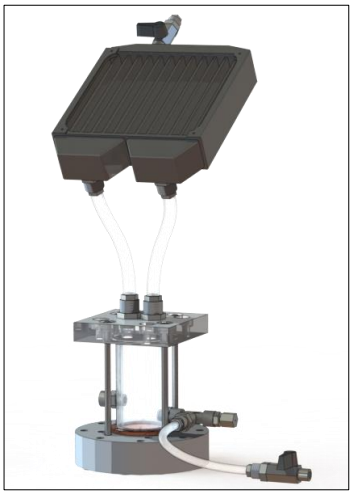
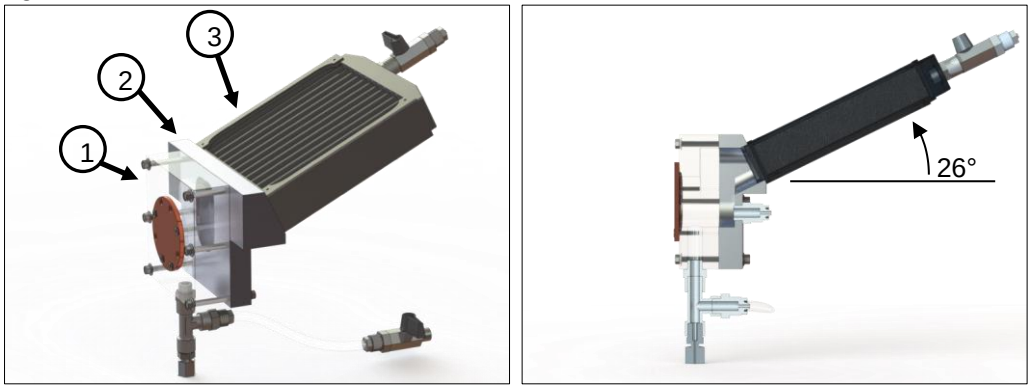


Figure 2.1 – Horizontally oriented prototype final design (CAD model).

2.2. Vertically oriented prototype facility

A potential configuration emerged as a one-body compact assembly of the condenser and evaporator into one integrated circulation chamber. This would further reduce the dimensions of the product to devise, being an important measure towards product development, considering the strong geometrical restrictions to install such a cooling device. In fact, since the cooler is intended for fitting on a CPU inside a computer, concerns regarding the available space inside the computer body were to be addressed, so a CAD model of the computer's interior was created, as a reference for the cooler's CAD assembly seen in figure 2.2:



a) b)

Figure 2.2 – Vertically oriented prototype final design. [a) Perspective view b) Midsection view. (CAD model)]

The three major components of the final assembly are (as seen in figure 2.2): (1) The evaporator body, where the boiling occurs; (2) The middle body, an interface between the evaporator and condenser; (3) The condenser, with further adaptations after it was used in the horizontally oriented facility.

3. Experimental setup

The experimental setup is schematically represented figure 3.1. It comprises the thermosyphon system in the bottom, being the main region of interest. Around it, the components which interact with it are represented: the transistor which simulates the heat release effect of a processor, the sensors (k-type

thermocouples and pressure transmitter) and the fan which forces convection on the thermosyphon condenser's fins to remove heat.

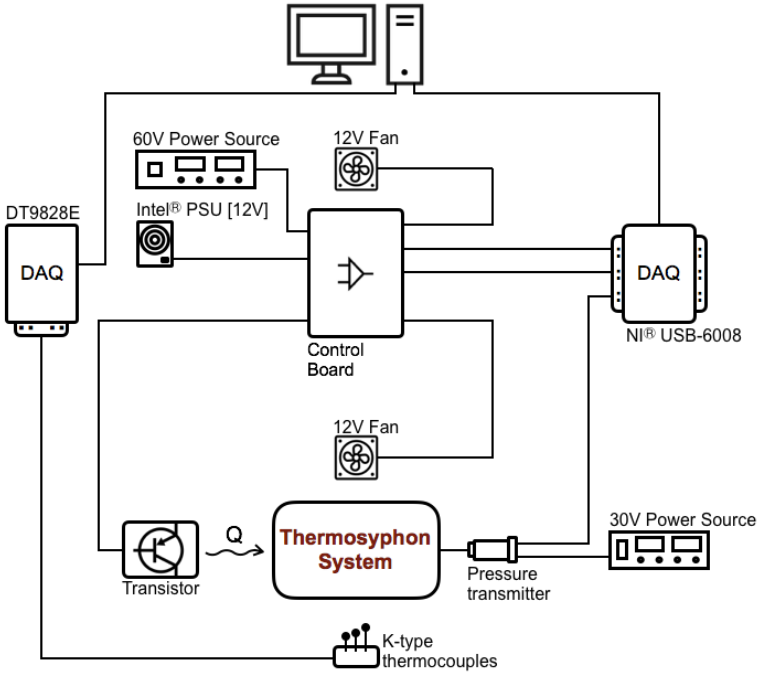
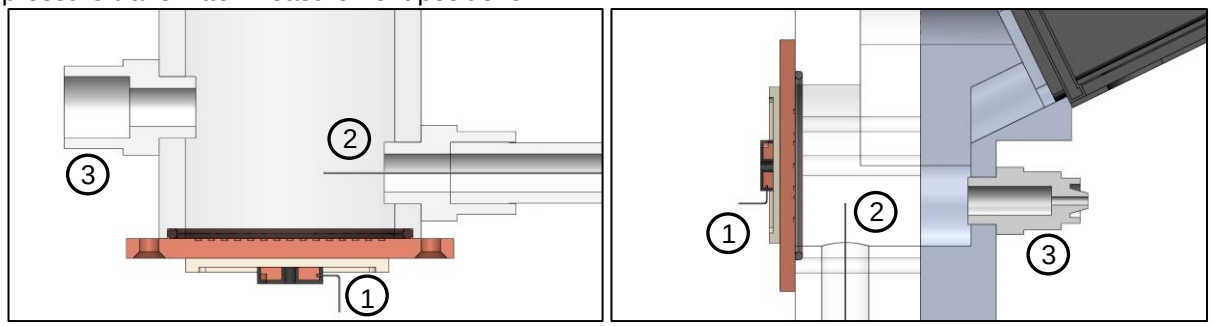


Figure 3.1 - Experimental setup with electronic control and acquisition system.

There are three thermocouples: one is placed in the region of the transistor's surface, to measure the copper surface to transistor junction temperature; the second is an insulated probe inserted inside the thermosyphon's evaporator, near the boiling side of the copper surface, to measure the saturation temperature in the system's closed chamber; the third is upstream to the condenser's fan forced convection air flow, to measure a reference ambient temperature to which heat is being removed. Figure 3.2 shows two midsection cuts of the horizontal and vertical facilities, clarifying the thermocouples and pressure transmitter measurement positions.



a) b)

Figure 3.2 - Horizontal and vertical facilities midsection cuts. [a) horizontal; b) vertical]

Number (1) is the first probe k-type thermocouple, used for measuring the junction temperature T_j, in the nearest available position, inside the transistor's own copper heat spreader. Number (2) is the second probe k-type thermocouple, used for obtaining the saturated vapour-liquid temperature, T_{sat} in the region near the hot surface, being placed 1 cm far from the later. Number (3) is the position of the accessory used to connect a small diameter pipe leading to the pressure transmitter. The thermocouples are manufactured by Omega®, two K-type calibration MTSS series probe thermocouples, and one surface thermocouple, SA1XL series. These thermocouples have an accuracy of ±1°C. The Analog to Digital Converter used for these thermocouples is a DT9828E by Data Translation®, with 24-bit conversion and an accuracy of 0,1 K. The pressure transmitter is manufactured by Gefran®. Its product model is TK-N-1-E-NO2U-M-V, with 0 to 10 Vdc output and -1 to 2 bar measurement range and has a ±0,5% FSO Typical accuracy. The two remaining components interacting with the thermosyhon, the transistor and fan, were control required so they are attached to an electronic control board developed within the scope of this work. Through this control board, signals from the computer converted to analog in the NI® DAQ board were sent to the fan to control its rotating speed and the transistor to control the power dissipated by Joule effect, as introduced next.

3.1. Electronic control

An electronic circuit which enables the imposition of the heat generated by the transistor, as well as the control of both the 12V computer fans was developed. Figure 3.3 displays a simplified scheme of the circuit and the connected transistor, related to its power control component.

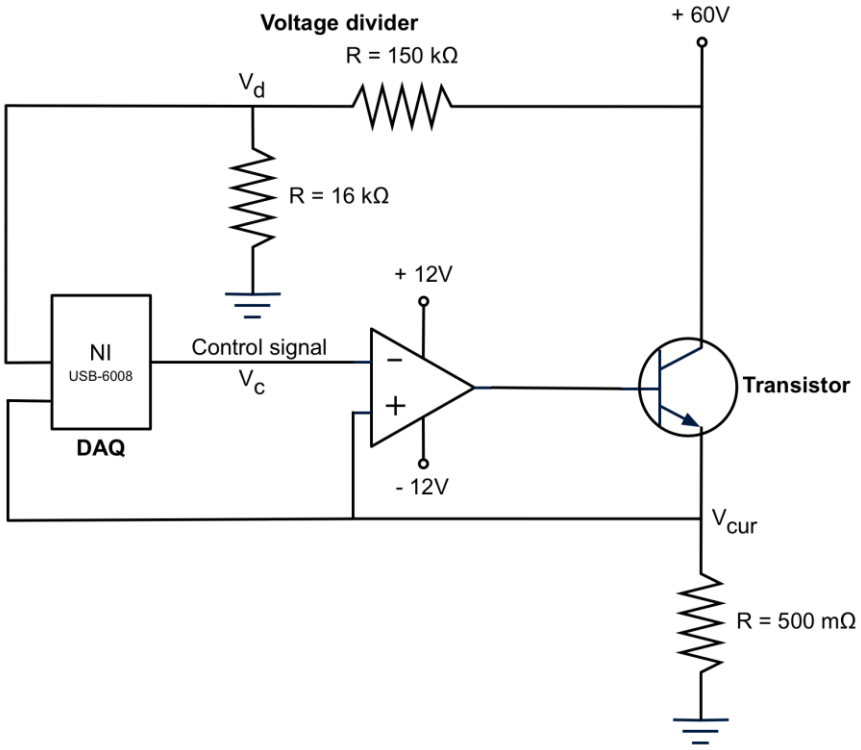


Figure 3.3 – Transistor power control circuit scheme.

The heat dissipated by Joule effect in the transistor is obtained as the product of the voltage drop across the transistor collector and emitter terminals and the current flowing through it, as seen in equation 3.1:

$$P_T = V_T * I_T \ [W] \tag{3.1}$$

which, replacing the voltage drop difference and Ohm's law current value is equivalent to

$$P_T = (V_{ps} - V_{cur}) * \frac{V_{cur}}{R} \ [W] \tag{3.2}$$

being V_{ps} the power source voltage and V_{cur} the voltage after the transistor. The op-amp in the scheme of figure 3.3 controls V_{cur} by comparing it to V_c, a control signal resulting of the LabVIEW program (as seen in section 3.2), where the user specifies the actual desired output power. With the op-amp causing the relation $V_{cur} = V_c$, one can now derive the expression to compute the control signal required to obtain a certain dissipated power value, P_T at the transistor:

$$P_T = \frac{V_{ps}V_{cur}}{R} - \frac{V_{cur}^2}{R} \Leftrightarrow V_{cur}^2 - V_{ps}V_{cur} + RP_T = 0 \tag{3.3}$$

Being the mathematical solution of the equation the following, with two solutions for any initial conditions, R, P_T and V_{ps}.

$$V_{cur} = \frac{V_{ps} \pm \sqrt{{V_{ps}}^2 - 4RP_T}}{2} \ [V] \tag{3.4}$$

As V_{cur} values bigger than V_{ps} lead to a negative heat load power, P_T, these values don't have a physical application to the current problem, being the final solution to the controlled voltage V_{cur} as follows:

$$V_{cur} = \frac{V_{ps} - \sqrt{{V_{ps}}^2 - 4RP_T}}{2} \ [V] \tag{3.5}$$

and for the current problem's conditions, with an actual measured resistance of $R = 502{,}82\ m\Omega$, and $V_{ps} = 60\ V$, V_{cur} in function of P_T comes as:

$$V_{cur}(P_T) = \frac{60 - \sqrt{3600 - 2{,}0113\ P_T}}{2} = 30 - \sqrt{900 - 0{,}5028\ P_T} \ [V] \tag{3.6}$$

3.2. Signal processing

A LabVIEW virtual instrument was developed in order to control the dissipated power to the transistor. Data processing was necessary, both to obtain the DAQ output power control signal V_c, as to accurately plot the remaining variables such as system pressure P, the computed transistor current I_c or the transistor computed dissipated power due to joule effect P_j. Figure 3.4 shows a scheme of the algorithm in which the LabVIEW block programming was based.

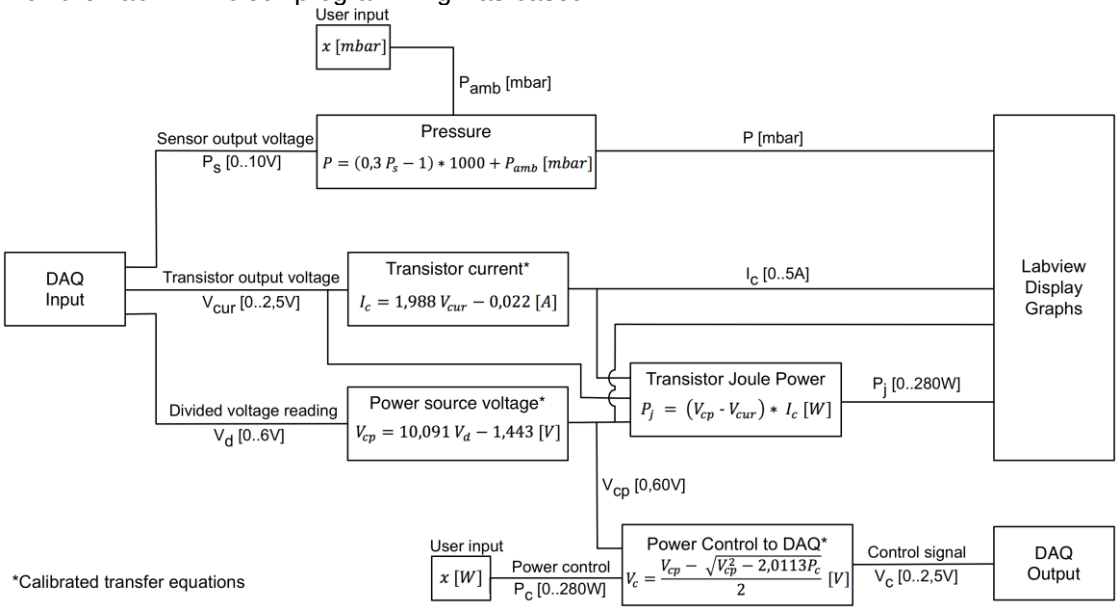


Figure 3.4 - LabVIEW visual programming algorithm diagram.

From the computed power source voltage, V_{cp} and the user defined transistor power value P_c, the control signal V_c is obtained through the adaptation of equation 3.5 for the current conditions, with $V_{ps} = V_{cp}$, $R = 502{,}82\ m\Omega$, and $V_{cur} = V_c$, resulting in:

$$V_c = \frac{V_{cp} - \sqrt{V_{cp}^2 - 2{,}0113 P_c}}{2}\ [V] \tag{3.7}$$

3.3. Experimental methodology

3.3.1. Steady-state conditions

For the surfaces' boiling curves to be obtained, measurements were taken when the thermosyphon pressure and temperature stabilized. An observation was the mean value of a 20 Hz AD conversion sample rate lasting 3 seconds, hence an average of 60 values. A full test is considered as the measurement points up to the occurrence of critical heat flux, or to a maximum safety value of 250W. In a CHF situation, a safety routine in the control system detects sudden temperature increases and immediately cuts the power source. Every surface is tested 5 times. The sequence is as follows, starting from a quiescent state: 5W steps from 0 to 40W; 10W steps from 40 to 250W or the occurrence of CHF. The first stage of 5W steps is for a more accurate observation of the transition regime from natural convection to nucleate boiling, with the appearance of the first bubbles.

3.3.2. Transient conditions

During transient observations, the interest is to register all variables as they change in time, so the observation time can be as long as the experiment states, or until a steady state is again attained. The experimental procedure can be described as follows: first, the system should be left to rest until it stabilizes at ambient conditions; data recording should then be started, followed by the triggering of any heat load step or combined step sequence for which the dynamic system response is sought; data recording should be stopped whenever temperature and pressure stabilize. Each surface was tested under five different transient scenarios: 20W, 60W, 100W and 140W power steps or a transient power profile adapted from the benchmark CPU power profile proposed by Isci and Martonosi [4], as depicted in figure 3.5:

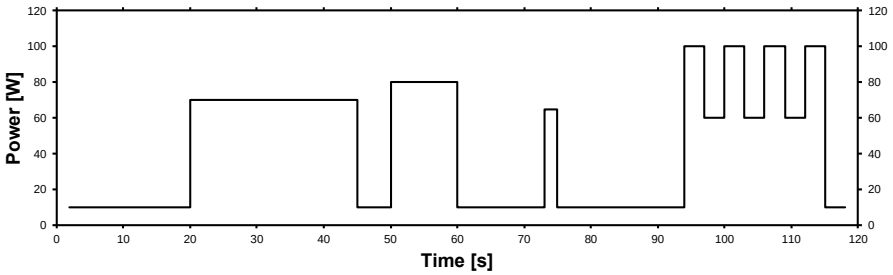


Figure 3.5 - Benchmark CPU power profile. [Adapted, [4]]

3.3.3. Real working conditions

For these tests to be performed, the factory-installed fan was carefully removed, allowing for the installation of the devised prototype to the CPU block. A system diagnostic and benchmarking software called AIDA64 Extreme was used to measure CPU core temperatures, the major variable of interest, as well as CPU load, fan speed and CPU consumed power. The software allowed access to its system diagnostic logs, which data was used to obtain the intended results. Furthermore, it contained a stress testing tool, used to obtain a transient thermal response after the sequenced activation and deactivation of its stress configuration which caused a 100% CPU load.

3.4. Uncertainty analysis

For the present work, three sources of uncertainty were identified, namely the following, as seen in table 1: (1) the pressure readings at the pressure transmitter and consecutive digital conversion in the respective DAQ board; (2) the temperature readings through the thermocouples and consecutive digital conversion in their respective DAQ board; (3) the heat load control, which implies voltage readings from the power source to the DAQ and, after the appropriate signal processing, digital to analog conversion for the power control signal to the Op-amp. Technical data on the associated instruments provided the following accuracy figures, for the present experimental setup configuration:

Table 1 - Accuracy data for featured instruments.

(1) Pressure readings		(2) Temperature readings		(3) Heat load control	
Transmitter	DAQ	Thermocouple	DAQ	AI*	AO*
0,5%	7,73 mV	± 1K	± 0,1K	7,73 mV	7 mV

(*) AI – Analog input; AO – Analog output.

4. Results and discussion

4.1. Steady-state cooling behavior analysis of surface structuration: horizontal orientation

Six different structured surfaces and a smooth reference surface were tested. They are classified according to a code based on their cavity distance parameter, *S*: surface 100 (*S* = 100 µm), 200, 400 and 600 with the addition of surfaces 200D (same as 200 with wider and deeper cavities) and 42T (hybrid concentric rings pattern with *S* = 400 and 200 µm). Figure 4.1 shows the obtained boiling curves for selected surfaces 42T, 400, 600 and the smooth. Error bars represent the surface junction temperature standard deviation from repeated experiments. It's very clear how the presence of surface structures alters the heat transfer dynamics, improving the dissipation of heat from the hot surface to the liquid, thus reducing the superheat temperature for every structured surface as compared to the smooth surface, for any heat flux value, up to the region of $2x10^5$ W/m^2. Horizontal dashed lines denote the two heat flux ranges of interest for the present study, 0,5 to $1,4x10^5$ W/m^2 and 1,6 to $2,5x10^5$ W/m^2, where different conditions were observed. Focusing in the lower range, where a nucleate boiling regime can be observed, there is a general trend for surfaces with lower *S* to attain lower values of surface junction superheat. This is clear comparing the surfaces 600 and 400 with the smooth surface. The structured surfaces' earlier transition from natural convection to nucleate regime (around $3x10^4$ W/m^2), as identified by the sudden slope increase, as compared to the smooth surface (around $6x10^4$ W/m^2) suggests the presence of cavities promotes an earlier onset of boiling, leading to improved cooling performance. At higher heat fluxes, a cyclical "choking" effect happens when liquid and vapour block each other's passage through the pipes connecting the evaporator and condenser. This causes large temperature fluctuations and sets an operating limit to the thermosyphon. Previous studies on reflux condenser setups [5]–[7], accounted for the same temperature fluctuation issues, arriving at similar conclusions regarding the cause for these fluctuations.

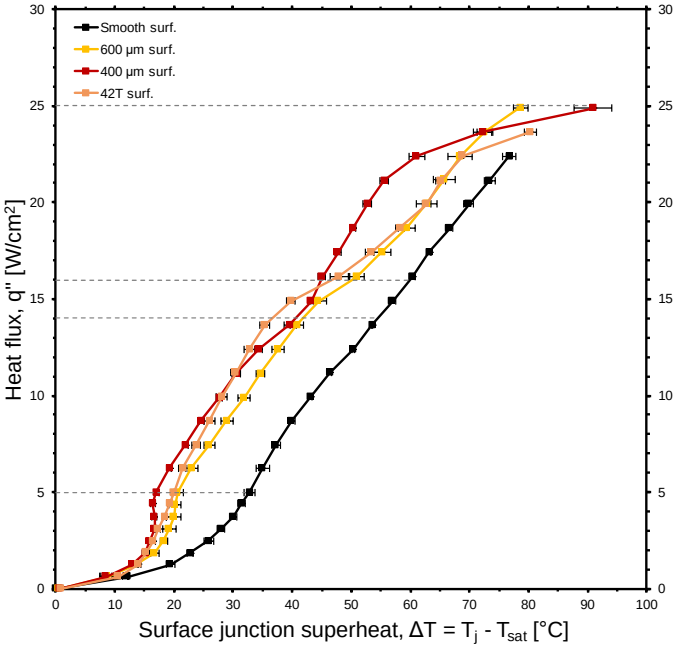
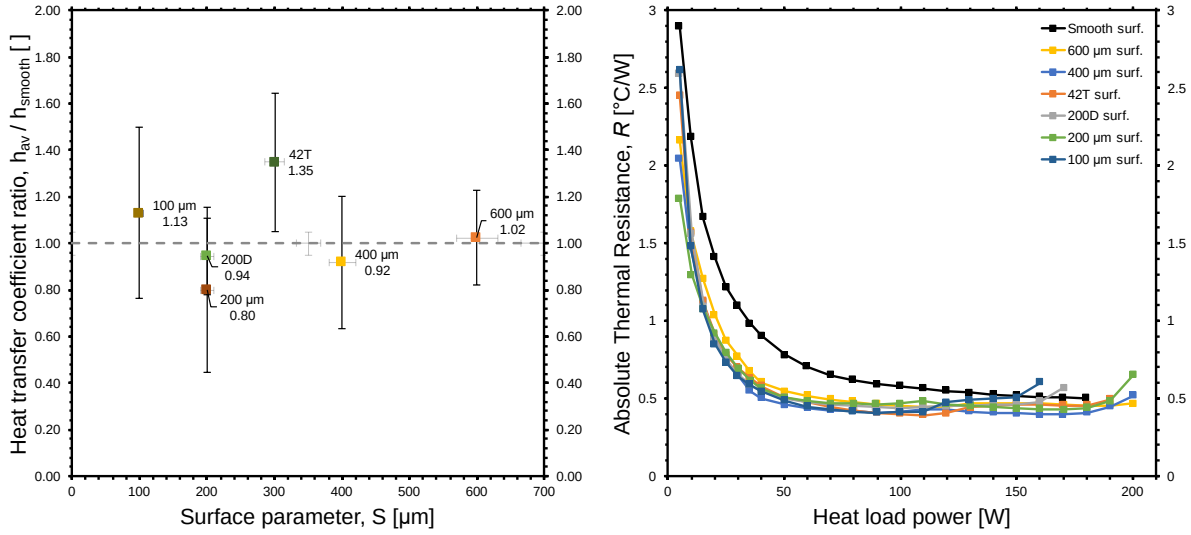


Figure 4.1 - Adapted boiling curves for surfaces 42T, 400, 600 and Smooth, with HFE-7000 as working fluid. [Horizontal]

Figure 4.2 shows the average heat transfer coefficients as computed over the first heat flux range of interest, 0,5 - 1,4x10^5 W/m^2, and the the average absolute thermal resistance, *R*, for each surface computed from junction to ambient temperature.



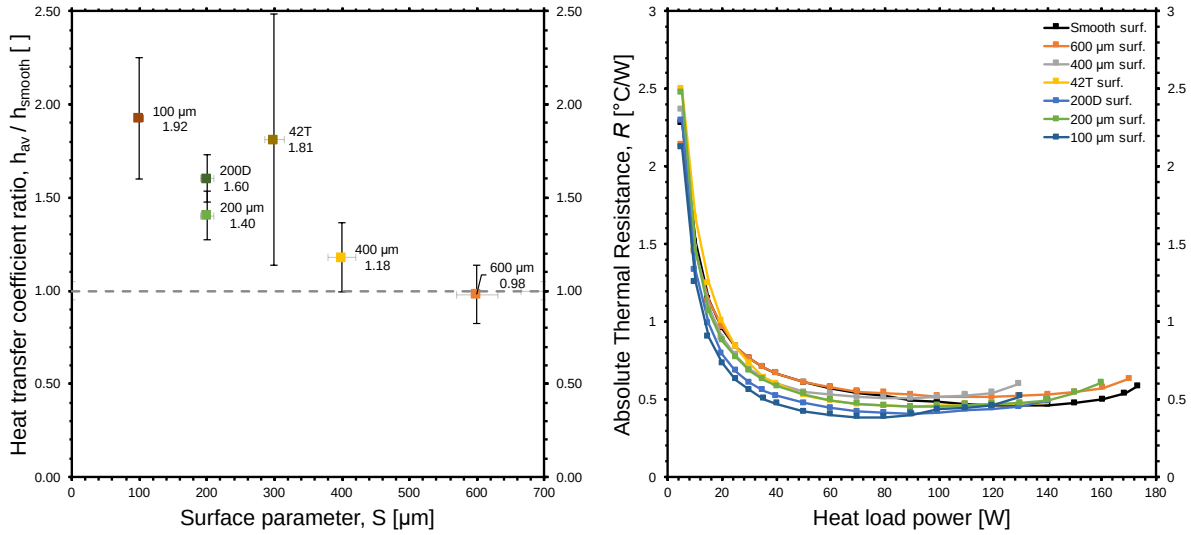
a) b)

Figure 4.2 – a) Structured to smooth surface average h ratios per surface parameter, *S*. b) Absolute thermal resistance, *R*, per surface. [Horizontal]

The smooth temperature shows the highest resistance, as expected, with surfaces 200, 100, 400 and 42T successively performing best regarding lowest resistance. According to figure 4.2.a) there is not an apparent trend for *h* improvement with the decrease of *S*, against previous observations by [3], [8], [9],. Possible causes can be the used experimental facility design was substantially different than previous setups, with the mentioned reflux condenser, for instance. Secondly, Moita et al. [8] and Valente et al. [10] refer that the shortening of distance between nucleation sites increases interaction mechanisms between departing bubbles, leading to their coalescence, which negatively affects boiling performance.

4.2. Steady-state cooling behavior analysis of surface structuration: vertical orientation

Following a similar approach as in the previous section, obtained results are as show in figure 4.3:



a) b)

Figure 4.3 - a) Structured to smooth surface average h ratios per surface parameter, *S*. b) Absolute thermal resistance, *R*, per surface. [Vertical]

The vertical orientation enabled a notorious *h* improvement for structured surfaces, and this time the predicted correlation between a reducing *S* parameter and an increasing *h* ratio is achieved, matching previous observations by [8], [9]. From a straight analysis, surfaces 100 and 42T seem to be the best performing in terms of *h* improvement. The wider and deeper cavities of surface 200D also enabled for an additional performance benefit compared to surface 200. Surface 100 again displays the lowest resistance through its entire heat load span, followed by surface 200D. Thermal resistance tends to increase by the very end of each curve, as the fully developed boiling regime got close to CHF, due to an issue with vertical bubble coalescence. To conclude, the final remark is that the most relevant or best performing surface for the vertical case is the one with *S* = 100 µm, which suggests further studies in vertical orientation should be carried through with smaller cavity distances.

4.3. Cooling behaviour under transient analysis: benchmark heat dissipation profile

Results obtained for the benchmark profile [4] are reported in figure 4.4, with power profile values plotted in the graph:

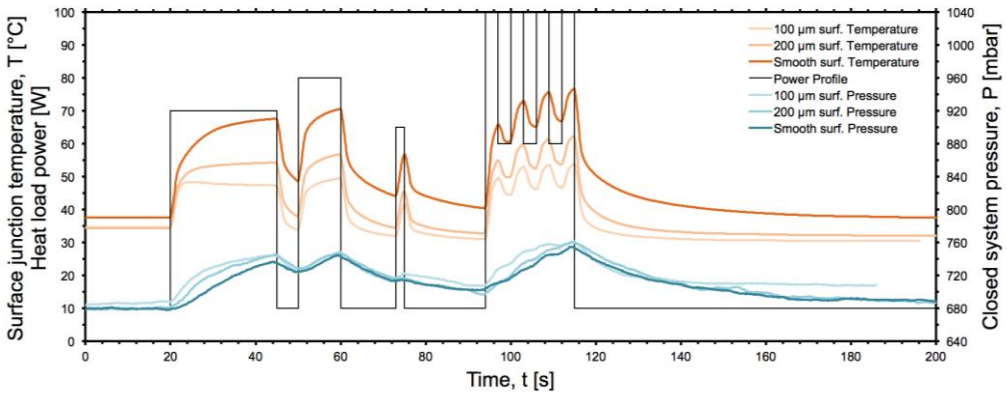


Figure 4.4 - Thermal and pressure response to an adapted power profile, for 3 selected surfaces.

Selected surfaces were 100, 200 and Smooth, being the first the best performing surface on previous section, 200 for comparison and inspection of cavity distance influence, and Smooth as a reference. Maximum allowed temperatures stand between 65 and 75°C for most commercial CPUs with standard clock speed operation, otherwise causing malfunction or breakdown. In the present scenario, the smooth surface could cause CPU malfunction, as its maximum temperature, achieved at around 114 s, was almost 80°C. Surface 100 would safely perform throughout all the cycle's timespan, with a maximum temperature of around 50°C.

4.4. Vertical prototype in real working conditions

As initially proposed, the developed vertical prototype was tested within its application purpose. It was inserted inside the desktop computer under study, and attached to its CPU unit, a QuadCore Intel® Core i7-2600K with 3600 MHz and Thermal design power, TDP = 95 W, with thermal compound between the prototype cooler's copper surface and the Integrated heat spreader of the processor, as common practice in the CPU cooling field. Figure 4.5 features a photograph of the obtained setup, with the cooler mounted on the CPU unit:

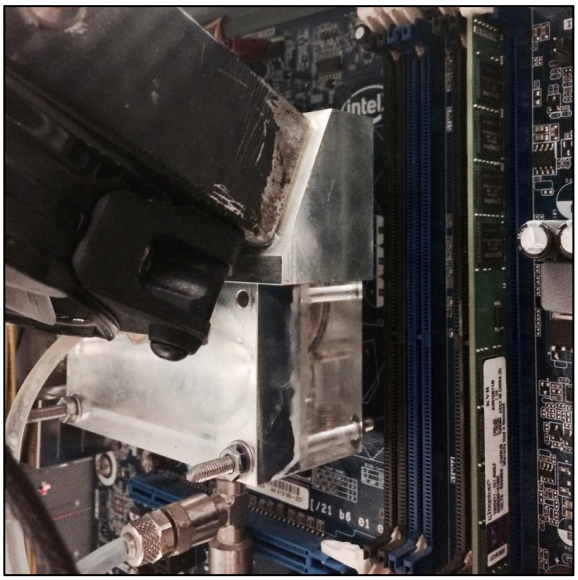


Figure 4.5 - Vertical prototype mounted on Intel motherboard.

With available resources, a transient analysis was performed to the CPU temperature response after an applied heat load profile. Software package AIDA64 for computer diagnosis and benchmark tests was used, additionally allowing for the reading and logging of every internal sensor in the computer, having been used to obtain the temperature values [°C], the CPU load [%], as well as fan rotating speeds [RPM] and the processor electric power [W]. Figure 4.6 shows the outcome of the described proceeding. The resulting CPU load profile varies, as mentioned, from idle to full load (stress test mode). The same profile was applied twice, with different equipped cooling technologies, the standard fan and this work's developed cooler. Results show a cooler temperature reduction of 12% for the fan maximum temperature, achieved around 00:09:00 time.

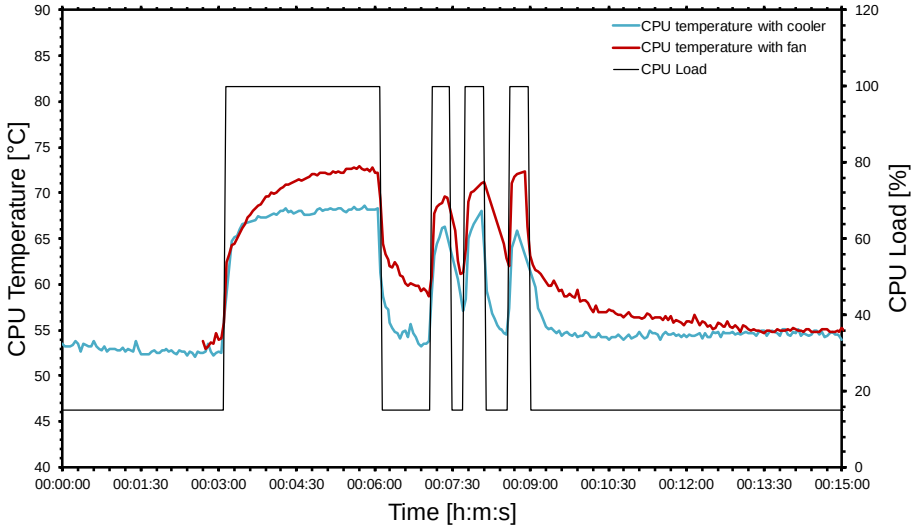


Figure 4.6 - Thermal response to an adapted heat load power profile in real CPU application.

In general, the cooling device presented a significant average 5°C temperature reduction at stress test, with the additional advantage of a lower system response time, which is very significant, since it allows for a faster reduction of temperature when the CPU goes back to idle. In the long term, this will improve the lifespan of the CPU unit, affected by continuous exposition to high temperatures.

5. Conclusions

The present work covers the test and optimization of an advanced microprocessor cooling product based on a two-phase closed loop thermosyphon, to operate under real conditions, meaning it was tested on a real computer CPU block. A dielectric liquid was used, HFE-7000, with the purpose of direct contact of the CPU's integrated heat spreader (or even its core) with the cooling liquid, in future optimization iterations. Besides having small to no environmental impact, this fluid also offers excellent thermal characteristics for the operating temperatures range of a typical modern CPU.
A horizontal and a vertical oriented cooling system were developed, analysed and extensively characterized. Steady-state results point the surface with S = 100 µm was the best performing. A study of the vertical prototype was performed in real conditions. It was attached to a real operating Intel® i7 processor and its thermal results at stress test were compared to the conventional air cooling fan core thermal behaviour, showing an average 5°C temperature reduction at stress test, with an additional lower system response time.

6. Acknowledgements

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7. References

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